STIC Search Report
EIC 2800

STIC Database Tracking Number: 101426

TO: Monica Lewis **Location:** **Art Unit : 2822** **Wednesday, August 20, 2003** **Case Serial Number: 09/998327**	**From: Bode Fagbohunka** **Location: EIC 2800** **CP4-9C18** **Phone: 703-605-1726** **bode.fagbohunka@uspto.gov**

Search Notes

Examiner Lewis,

Please find attached the results of your search for 09/998327. The search was conducted using the standard collection of databases on dialog for EIC 2800. The tagged references appear to be the closest references located during our search.

If you would like a re-focus please let me know or if you have any questions regarding the search results please do not hesitate to contact me.

Bode Fagbohunka

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Set     Items   Description
S1     252838   (BOND? OR TENSILE)(3N)(STRENGTH OR ATTACH? OR CONNECT?)
S2     768011   THERMOSET?(3N)RESIN?  OR EPOXY OR ANIMIDE OR POLYIMIDE OR -
             ARAMID OR LIQUID()CRYSTAL()POLYMER? OR PREPREG? ? OR (PHENOL -
             OR NAPHTHALENE OR UREA OR AMINO OR ALKYD OR SILICON? ? OR FUR-
             AN OR POLYESTER OR POLYURETHANE)(2N)RESIN?
S3     290267   (INSULAT? OR WIR????)(3N)(BASE? OR LAYER? OR REGION? OR SE-
             CTION?)
S4        511   S1 AND S2 AND S3
S5         32   S1(6N)S2(6N)S3
S6         32   RD (unique items)
S7         23   S6 AND PY<=2000
? show files
File 315:ChemEng & Biotec Abs 1970-2003/Jul
         (c) 2003 DECHEMA
File   2:INSPEC 1969-2003/Aug W2
         (c) 2003 Institution of Electrical Engineers
File   6:NTIS 1964-2003/Aug W3
         (c) 2003 NTIS, Intl Cpyrght All Rights Res
File   8:Ei Compendex(R) 1970-2003/Aug W2
         (c) 2003 Elsevier Eng.  Info. Inc.
File  34:SciSearch(R) Cited Ref Sci 1990-2003/Aug W2
         (c) 2003 Inst for Sci Info
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File  99:Wilson Appl. Sci & Tech Abs 1983-2003/Jul
         (c) 2003 The HW Wilson Co.
File  94:JICST-EPlus 1985-2003/Aug W2
         (c)2003 Japan Science and Tech Corp(JST)
File  35:Dissertation Abs Online 1861-2003/Jul
         (c) 2003 ProQuest Info&Learning
File  65:Inside Conferences 1993-2003/Aug W3
         (c) 2003 BLDSC all rts. reserv.
File 144:Pascal 1973-2003/Aug W2
         (c) 2003 INIST/CNRS
File 347:JAPIO Oct 1976-2003/Apr(Updated 030804)
         (c) 2003 JPO & JAPIO
File 350:Derwent WPIX 1963-2003/UD,UM &UP=200353
         (c) 2003  Thomson Derwent
?
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7/9/10 **(Item 7 from file: 347)**
DIALOG(R)File 347:JAPIO

03696094 **Image available**
MANUFACTURE OF METAL-BASED WIRING BOARD

PUB. NO.: 04-061194 [JP 4061194 A]
PUBLISHED: February 27, 1992 (**19920227**)
INVENTOR(s): MIYAZAKI MAKOTO
NISHIYAMA KATSUMI
MUNEMURA KUNITSUGU
IMAGAWA SHUNJIRO
OBAYASHI SOICHI
APPLICANT(s): MURATA MFG CO LTD [000623] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-165335 [JP 90165335]
FILED: June 22, 1990 (19900622)
INTL CLASS: [5] H05K-003/44; B32B-015/08; H05K-003/18
JAPIO CLASS: 42.1 (ELECTRONICS -- Electronic Components); 14.2 (ORGANIC CHEMISTRY -- High Polymer Molecular Compounds)
JAPIO KEYWORD:R124 (CHEMISTRY -- Epoxy Resins)
JOURNAL: Section: E, Section No. 1216, Vol. 16, No. 263, Pg. 104, June 15, 1992 (19920615)

ABSTRACT

PURPOSE: To improve the thermal conductivity of an **insulating layer** by increasing **bonding strength** between an electroless plating **layer** and the **insulating layer** by forming the **insulating layer** after applying an **epoxy** resin material containing a high heat conduction inorganic filler on a surface of a metal base using a doctor blade, and thereafter roughening the surface to from an electroless plating layer.

CONSTITUTION: An insulating layer 3 is formed by applying an insulating layer material containing epoxy resin as a chief ingredient on a surface of a metal base 2 using a doctor blade. To the epoxy resin an aluminum oxide and an aluminum nitride both being a high heat conduction inorganic filler are added by 30% by weight or more and 80% by weight or less. Then, a resist film 4 having an opening 5 of the same pattern as a circuit pattern is formed, and the surface of an exposed part of the insulating layer 3 is roughened and subjected to copper electroless plating to form an electroless plating layer 6. Then, after washing and drying the resist film 4 is removed by trichloroethane to yield a circuit pattern conductor circuit 7

7/9/6 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

05867148 **Image available**
WIRING BOARD AND ITS MANUFACTURE

PUB. NO.: 10-150248 [JP 10150248 A]
PUBLISHED: June 02, 1998 (**19980602**)
INVENTOR(s): SHIKADA HIDENORI
FUJII SHUNICHI
APPLICANT(s): KYOCERA CORP [358923] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-308158 [JP 96308158]
FILED: November 19, 1996 (19961119)
INTL CLASS: [6] H05K-001/02
JAPIO CLASS: 42.1 (ELECTRONICS -- Electronic Components); 14.2 (ORGANIC CHEMISTRY -- High Polymer Molecular Compounds)
JAPIO KEYWORD:R031 (METALS -- Powder Metallurgy); R124 (CHEMISTRY -- Epoxy Resins)

ABSTRACT

PROBLEM TO BE SOLVED: To strengthen the **bonding strength** of wiring conductors to an **insulating base** body by a method wherein an intermediate layer consisting of a **thermosetting resin** is made to interpose between the insulating base body and the wiring conductors and at the same time, the thermosetting resin of the intermediate layer is bonded to the thermosetting resin of each of the insulating base body and the wiring conductors by a crosslinking reaction.

SOLUTION: An intermediate layer is made to interpose between wiring conductors 2 and the upper surface of an insulating substrate 1b constituting an insulating base body 1. The thermosetting resin of the intermediate layer causes a crosslinking reaction with the thermosetting resin of each of the substrate 1b and the wiring conductors 2, whereby the wiring conductors 2 are firmly bonded to the substrate 1b. Thereby, when electrodes on a semiconductor element 3 are connected with the conductors 2 via bonding wires 4 or at other times, the conductors 2 are never separated from the base body 1 (the surface of the substrate 1b) by an external force even if the large external force is applied to the conductors 2. Thereby, it becomes possible to connect electrically each electrode on the element 3 with each wiring conductor 2 reliably and firmly

7/9/15 **(Item 12 from file: 347)**
DIALOG(R)File 347:JAPIO

00810645 **Image available**
COUPLING AGENT BETWEEN INORGANIC INSULATING FILM WITH SILICON AND POLYIMIDE RESIN FILM

PUB. NO.: 56-130945 [JP 56130945 A]
PUBLISHED: October 14, 1981 (**19811014**)
INVENTOR(s): KOKUNI NAOYUKI
FUJIEDA SHINETSU
SUZUKI SHIYUICHI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 55-033443 [JP 8033443]
FILED: March 18, 1980 (19800318)
INTL CLASS: [3] H01L-021/88; C09D-003/49; C09D-005/00; C09J-003/00; H01L-021/31; H01L-023/30
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components); 14.2 (ORGANIC CHEMISTRY -- High Polymer Molecular Compounds); 14.7 (ORGANIC CHEMISTRY -- Coating Material Adhesives)
JAPIO KEYWORD:R119 (CHEMISTRY -- Heat Resistant Resins)
JOURNAL: Section: E, Section No. 90, Vol. 06, No. 9, Pg. 33, January 20, 1982 (19820120)

ABSTRACT

PURPOSE: To prevent the corrosion of a wiring layer with a coupling agent for enhancing the adherence between a semiconductor substrate and a polyimide resin film by forming the agent of silico-aluminate ester compound and organic solvent and retaining the mixture amount constantly.

CONSTITUTION: A silico-aluminate ester compound is formed by the formula represented by (R(sub 1)O)(sub 2)Al-O-Si(OR(sub 2))(sub 2), where the R(sub 1), R(sub 2) may be the same or different, and signify 1-4C alkyl group. The mixture ratio of the silico-aluminate ester compound should be in the range of 0.01-50wt%. The coupling agent 4 is interposed between a silicon dioxide film 2 on the substrate 1 and aluminum **wiring layer** 3, **polyimide** resin film 5. Thus, the **bonding strength** of the respective materials become uniform, and it can prevent the entrance of water content for corroding the aluminum wiring layer.

7/9/18 **(Item 2 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

011695263 **Image available**
WPI Acc No: 1998-112173/ **199811**
XRAM Acc No: C98-036886
XRPX Acc No: N98-089893
Pneumatic tyre without bead wires - has beads containing annular element, of tensile strength **less than equivalent bead** wire **and reinforcing** layers **around it of** tensile strength **greater than equivalent bead wire, preferably made of** aramid
Patent Assignee: CIE GEN ETAB MICHELIN & CIE (MICL); MICHELIN & CIE (MICL)
Inventor: AHOUANTO M; EYNARD C; PEYROT A
Number of Countries: 026 Number of Patents: 011
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 823341	A1	19980211	EP 97113305	A	19970801	199811	B
AU 9733212	A	19980212	AU 9733212	A	19970807	199814	
FR 2752200	A1	19980213	FR 9610187	A	19960809	199814	
JP 10071815	A	19980317	JP 97227423	A	19970808	199821	
CA 2211576	A	19980209	CA 2211576	A	19970805	199829	
BR 9705122	A	19980908	BR 975122	A	19971023	199842	
KR 98018520	A	19980605	KR 9737935	A	19970808	199922	
US 5961756	A	19991005	US 97903841	A	19970731	199948	
AU 723501	B	20000831	AU 9733212	A	19970807	200046	
CN 1173434	A	19980218	CN 97116716	A	19970808	200170	
RU 2196686	C2	20030120	RU 97113749	A	19970808	200320	

Priority Applications (No Type Date): FR 9610187 A 19960809
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 823341	A1	F	13	B60C-015/00	
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
AU 9733212	A			B60C-001/00	
FR 2752200	A1		24	B60C-015/00	
JP 10071815	A		9	B60C-015/04	
CA 2211576	A			B60C-015/00	
BR 9705122	A			B60C-009/02	
KR 98018520	A			B60C-015/00	
US 5961756	A			B60C-015/00	
AU 723501	B			B60C-001/00	Previous Publ. patent AU 9733212
CN 1173434	A			B60C-009/00	
RU 2196686	C2			B60C-015/04	

Abstract (Basic): EP 823341 A

A tyre has no bead wires but each bead presents (a) an annular element (7) with a longitudinal tensile strength significantly less than that needed for a bead wire of an equivalent sized tyre; (b) at least two layers of reinforcement (8, 9, 10) placed in contact or in proximity to the annular element, where each reinforced layer consists of parallel strands but the strands of adjacent layers are displaced by an angle of up to 10 deg. ; (c) the assembly of reinforcing layers has ultimate tensile strength at least equal to that necessary for a traditional bead wire; (d) the carcass layers are wound around the annular element; and (e) the outer area of the bead has a rubber with a modulus of elastic loss G'' less than 1 MPa and/or the thickness of the rubber is at most 2 mm.

USE - Tyre bead production.

ADVANTAGE - Improves ease of production and endurance of the tyre

due to lowered hysteresis losses.
Dwg.2/5
Title Terms: PNEUMATIC; TYRE; BEAD; WIRE; BEAD; CONTAIN; ANNULAR; ELEMENT; TENSILE; STRENGTH; LESS; EQUIVALENT; BEAD; WIRE; REINFORCED; LAYER; TENSILE; STRENGTH; GREATER; EQUIVALENT; BEAD; WIRE; PREFER; MADE; ARAMID
Derwent Class: A95; Q11
International Patent Class (Main): B60C-001/00; B60C-009/00; B60C-009/02; B60C-015/00; B60C-015/04
International Patent Class (Additional): B60C-009/04; B60C-009/10; B60C-015/06
File Segment: CPI; EngPI
Manual Codes (CPI/A-N): A12-T01B
Polymer Indexing (PS):
<01>
001 018; H0124-R
002 018; ND01; Q9999 Q9256-R Q9212; N9999 N7261; B9999 B4171 B4091 B3838 B3747; K9892; B9999 B4002 B3963 B3930 B3838 B3747
003 018; A999 A419; S9999 S1070-R; S9999 S1672
<02>
001 018; P0737-R P0635 H0293 F70 D01 D18; S9999 S1070-R; A999 A419; A999 A782; S9999 S1672

7/9/22 **(Item 6 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

009208909 **Image available**
WPI Acc No: 1992-336331/ **199241**
XRPX Acc No: N92-256499
Semiconductor device with ceramic substrate to increase patterning accuracy and wire bonding stability - forms polyimide **film on entire** region **except die** attached wire bonding regions **and forms copper@ or aluminium@ film by vapour phase and then conducts pattern etching NoAbstract**
Patent Assignee: HITACHI CABLE LTD (HITD)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 4240752	A	19920828	JP 917656	A	19910125	199241	B

Priority Applications (No Type Date): JP 917656 A 19910125
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 4240752	A		4	H01L-023/12	

Title Terms: SEMICONDUCTOR; DEVICE; CERAMIC; SUBSTRATE; INCREASE; PATTERN; ACCURACY; WIRE; BOND; STABILISED; FORM; POLYIMIDE; FILM; REGION; DIE; ATTACH; WIRE; BOND; REGION; FORM; COPPER; ALUMINIUM; FILM; VAPOUR; PHASE; CONDUCTING; PATTERN; ETCH; NOABSTRACT
Derwent Class: U11
International Patent Class (Main): H01L-023/12
International Patent Class (Additional): H01L-021/60
File Segment: EPI
Manual Codes (EPI/S-X): U11-D01A; U11-D03A2; U11-D03B3; U11-E01A

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Set     Items   Description
S1      81451   AU=(TOMEKAWA S? OR TOMEKAWA, S? OR YAMASHITA Y? OR YAMASHI-
             TA, Y? OR SUZUKI T? OR SUZUKI, T? OR KAWAKITA Y? OR KAWAKITA,
             Y? OR NAKAMURA T? OR NAKAMURA, T?)
S2     156855   (BOND? OR TENSILE)(3N)(STRENGTH OR ATTACH? OR CONNECT?)
S3        477   S1 AND S2
S4     640698   THERMOSET?(3N)RESIN?  OR EPOXY OR ANIMIDE OR POLYIMIDE OR -
             ARAMID OR LIQUID()CRYSTAL()POLYMER? OR PREPREG? ? OR (PHENOL -
             OR NAPHTHALENE OR UREA OR AMINO OR ALKYD OR SILICON? ? OR FUR-
             AN OR POLYESTER OR POLYURETHANE)(2N)RESIN
S5        102   S4 AND S3
S6     311165   ( INSULAT? OR WIR????)(3N)(BASE? OR LAYER? OR REGION? OR S-
             ECTION)
S7         15   S5 AND S6
S8         15   IDPAT (sorted in duplicate/non-duplicate order)
S9         14   IDPAT (primary/non-duplicate records only)
?  show files
File 344:Chinese Patents Abs Aug 1985-2003/Mar
         (c) 2003 European Patent Office
File 347:JAPIO Oct 1976-2003/Apr(Updated 030804)
         (c) 2003 JPO & JAPIO
File 348:EUROPEAN PATENTS 1978-2003/Aug W02
         (c) 2003 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20030814,UT=20030807
         (c) 2003 WIPO/Univentio
File 350:Derwent WPIX 1963-2003/UD,UM &UP=200353
         (c) 2003  Thomson Derwent
?
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9/9/13 **(Item 13 from file: 347)**
DIALOG(R)File 347:JAPIO

07543504 **Image available**
CIRCUIT DEVICE AND ITS MANUFACTURING METHOD

PUB. NO.: 2003-037344 [JP 2003037344 A]
PUBLISHED: February 07, 2003 (20030207)
INVENTOR(s): SAKAMOTO NORIAKI
IGARASHI YUUSUKE
NAKAMURA TAKESHI
KOBAYASHI YOSHIYUKI
APPLICANT(s): SANYO ELECTRIC CO LTD
APPL. NO.: 2001-225107 [JP 20011225107]
FILED: July 25, 2001 (20010725)
INTL CLASS: H05K-001/18; H01L-023/12; H01L-025/00; H05K-001/02; H05K-001/11; H05K-003/00; H05K-003/06; H05K-003/24; H05K-003/28; H05K-003/32

ABSTRACT

PROBLEM TO BE SOLVED: To solve the problem of a circuit device employing a ceramic substrate, a flexible sheet, or the like, as a supporting substrate for mounting circuit elements that a manufacturing method exhibiting high mass productivity is not yet established when the size and thickness of the circuit device are reduced.

SOLUTION: The circuit device comprises a plurality of conductive patterns 51 at respective mounting parts isolated electrically by isolation trenches 61, a **thermosetting resin** layer 50A covering the surface of the conductive patterns 51 while filling the isolation trenches 61, and an insulating resin 50B bonded to the **thermosetting resin** layer 50A while covering a circuit element 52 wherein **bonding strength** is enhanced between the isolation trench 61 and the **thermosetting resin layer** 50A and the **insulating** resin 50B, and the coupling parts of a conductive foil 60 provided with no isolation trench 61 are used as outer electrodes 56A, 56B and 56C.

?

9/9/12 **(Item 12 from file: 347)**
DIALOG(R)File 347:JAPIO

07543505 **Image available**
CIRCUIT DEVICE AND ITS MANUFACTURING METHOD

PUB. NO.: 2003-037345 [JP 2003037345 A]
PUBLISHED: February 07, 2003 (20030207)
INVENTOR(s): SAKAMOTO NORIAKI
IGARASHI YUUSUKE
NAKAMURA TAKESHI
KOBAYASHI YOSHIYUKI
APPLICANT(s): SANYO ELECTRIC CO LTD
APPL. NO.: 2001-225108 [JP 20011225108]
FILED: July 25, 2001 (20010725)
INTL CLASS: H05K-001/18; H01L-023/12; H05K-001/02; H05K-001/11; H05K-003/00; H05K-003/06; H05K-003/24; H05K-003/28; H05K-003/32

ABSTRACT

PROBLEM TO BE SOLVED: To solve the problem of a circuit device employing a ceramic substrate, a flexible sheet, or the like, as a supporting substrate for mounting circuit elements that a manufacturing method exhibiting high mass productivity is not yet established when the size and thickness of the circuit device are reduced.

SOLUTION: The circuit device comprises a plurality of conductive patterns 51 at respective mounting parts isolated electrically by isolation trenches 61, a **thermosetting resin** layer 50A covering the surface of the conductive patterns 51 while filling the isolation trenches 61, and an insulating resin 50B bonded to the **thermosetting resin** layer 50A while covering a circuit element 52 wherein **bonding strength** is enhanced between the isolation trench 61 and the **thermosetting resin layer** 50A and the **insulating** resin 50B, and the conductive pattern can also be arranged beneath the circuit element 52.

9/9/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2003 Thomson Derwent. All rts. reserv.

014821257
WPI Acc No: 2002-641963/200269
XRAM Acc No: C02-181268
XRPX Acc No: N02-507373
Circuit substrate for semiconductor device, in which bonding strength **between** wiring layer **and** insulating base **is lesser than that between** wiring layer **and conductor arranged inside** insulating base

Patent Assignee: MATSUSHITA ELECTRIC IND CO LTD (MATU); MATSUSHITA DENKI SANGYO KK (MATU)
Inventor: **KAWAKITA Y** ; **NAKAMURA T** ; **SUZUKI T** ; **TOME**KAWA S ; **YAMASHITA Y**
Number of Countries: 029 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020066961	A1	20020606	US 2001998327	A	20011203	200269	B
EP 1213952	A2	20020612	EP 2001128763	A	20011203	200269	
JP 2002237677	A	20020823	JP 2001364225	A	20011129	200271	
CN 1364049	A	20020814	CN 2001142893	A	20011205	200280	

Priority Applications (No Type Date): JP 2000370406 A 20001205
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020066961	A1		24	H01L-023/48	
EP 1213952	A2	E		H05K-003/40	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR					
JP 2002237677	A		15	H05K-003/38	
CN 1364049	A			H05K-001/00	

Abstract (Basic): US 20020066961 A1
NOVELTY - The circuit substrate has **wiring layers** on an **insulating base** . A conductor containing **thermosetting resin** is arranged inside the **insulating base** , to electrically connect the **wiring layers** of the **insulating base** . The **bonding strength** between the **wiring layer** and **insulating base** is set lesser than that between the **wiring layer** and the conductor.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for circuit substrate manufacturing method.
USE - Circuit substrate for semiconductor device.
ADVANTAGE - Ensures high connection reliability even under high temperature cycle, by increasing **bonding strength** between **wiring layers** and conductor.
pp; 24 DwgNo 0/13
Title Terms: CIRCUIT; SUBSTRATE; SEMICONDUCTOR; DEVICE; BOND; STRENGTH; WIRE; LAYER; INSULATE; BASE; WIRE; LAYER; CONDUCTOR; ARRANGE; INSULATE; BASE
Derwent Class: A85; L03; V04
International Patent Class (Main): H01L-023/48; H05K-001/00; H05K-003/38; H05K-003/40
International Patent Class (Additional): H05K-001/02; H05K-003/46
File Segment: CPI; EPI
Manual Codes (CPI/A-N): A12-E07C; L03-H04E3
Manual Codes (EPI/S-X): V04-Q05
Polymer Indexing (PS):
<01>

001 018; P0464-R D01 D22 D42 F47; H0328
002 018; ND01; ND07; Q9999 Q7476 Q7330; Q9999 Q7454 Q7330; K9676-R;
B9999 B5618 B5572; Q9999 Q7818-R; N9999 N7192 N7023; N9999 N5721-R;
Q9999 Q6644-R; B9999 B5618 B5572; N9999 N6177-R; B9999 B5301 B5298
B5276; K9461; B9999 B4171 B4091 B3838 B3747; K9483-R
003 018; A999 A135; S9999 S1514 S1456
004 018; A999 A157-R; S9999 S1514 S1456

9/9/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01581697
Piezoelectric transducer, manufacturing method of piezoelectric transducer and pulse wave detector
Piezoelektrischer Wandler, zugehoriges Herstellungsverfahren und Pulswellenaufnehmer
Transducteur piezoelectrique, son procede de fabrication et detecteur d'onde d'impulsion

PATENT ASSIGNEE:
SEIKO INSTRUMENTS INC., (839492), 8 Nakase 1-chome, Mihama-ku, Chiba-shi, Chiba 261, (JP), (Applicant designated States: all)
INVENTOR:
Hiroyuki Muramatsu., c/o Seiko Instruments Inc., 8 Nakase 1-chome, Mihama-ku, Chiba-shi, Chiba, (JP)
Shinogi Masataka., c/o Seiko Instruments Inc, 8 Nakase 1-chome, Mihama-ku , Chiba-shi, Chiba, (JP)
Nakamura Takashi., c/o Seiko Instruments Inc. , 8 Nakase 1-chome, Mihama-ku, Chiba-shi, Chiba, (JP
LEGAL REPRESENTATIVE:
Kenyon, Sarah Elizabeth et al (62343), Miller Sturt Kenyon 9 John Street, London WC1N 2ES, (GB)
PATENT (CC, No, Kind, Date): EP 1312424 A2 030521 (Basic)
APPLICATION (CC, No, Date): EP 2002257892 021115;
PRIORITY (CC, No, Date): JP 2001352140 011116
DESIGNATED STATES: AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE; SK; TR
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: B06B-001/06

ABSTRACT EP 1312424 A2
With respect to a conventional and general supersonic probe, it is necessary to apply a special patterning to a piezoelectric element, so that this involves a problem such that the supersonic probe is difficult to manufacture. Alternatively, in the case of bonding the conducting wire to the piezoelectric element with the conductive adhesive or the like, it is necessary to make the thickness of the conductive adhesive and the thickness of the conductive wire less than or equal to that of the above mentioned acoustic matching layer, so that it is very difficult to manufacture and the thickness of the acoustic matching layer becomes thicker than the optimum thickness. This involves a problem such that the detection sensitivity has been deteriorated. In order to solve the above described problems, a piezoelectric transducer (4) according to the present invention is constructed in a laminated layer such that a piezoelectric element (41,43), to which electrodes (52, 53) are provided at the opposite surfaces, is fixed on a substrate (43) having a plurality of substrate electrodes (47b) and further, an acoustic matching layer (49) for efficiently transmitting and receiving a supersonic wave is superposed on the above mentioned piezoelectric element. Additionally, one surface electrode among the surface electrodes, which are respectively provided on the opposite surfaces of the above mentioned piezoelectric element, is connected to the above mentioned substrate electrodes with conductivity as superimposed with each other and other surface electrode is connected to the above mentioned substrate electrodes with conductivity via the conductive member and further, other surface electrode has a connection structure such that the above mentioned conductive member is connected thereto within the thickness of the acoustic matching layer without being exposed.
ABSTRACT WORD COUNT: 283

NOTE:
Figure number on first page: 5

LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 030521 A2 Published application without search report
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200321	818
SPEC A	(English)	200321	6863
Total word count - document A			7681
Total word count - document B			0
Total word count - documents A + B			7681

SPECIFICATION EP 1312424 A2

The present invention relates to a piezoelectric transducer and specifically, the present invention relates to a piezoelectric transducer, a manufacturing method of the piezoelectric transducer and a pulse wave detector for detecting the information of the interior of a human body and the interior of an object.

A conventional piezoelectric transducer to be used as a supersonic probe or the like will be explained with reference to FIGS. 16, 17 and 18.

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SEMICONDUCTOR PACKAGE, SEMICONDUCTOR DEVICE, ELECTRONIC DEVICE AND PRODUCTION METHOD FOR SEMICONDUCTOR PACKAGE

HALBLEITERGEHAUSE, HALBLEITER, ELEKTRONIKELEMENT UND HERSTELLUNG EINES HALBLEITERGEHAUSES

BOITIER A SEMI-CONDUCTEUR, DISPOSITIF SEMI-CONDUCTEUR, DISPOSITIF ELECTRONIQUE ET PROCEDE DE FABRICATION DE BOITIER A SEMI-CONDUCTEUR

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ABSTRACT EP 1107306 A1

An **insulating layer** (3) is formed on a Si wafer (1). An opening portion is made in this **insulating layer** (3), and subsequently a rerouting layer (2) is formed. Next, a resin layer (4) is formed on the rerouting layer (2). The resin layer (4) is then cured so that the rerouting layer (2) and a Cu foil (5) are bonded to each other through the resin layer (4). Thereafter, a ring-like opening portion (4a) is made in the resin layer (4), and a Cu plating layer (8) is formed inside this opening portion (4a).

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SPECIFICATION EP 1107306 A1

Technical Field

The present invention relates to a semiconductor package, such as a wafer level CSP (Chip Size/Scale Package), using no wiring board (interposer), a semiconductor device, an electronic device, and a method for producing the semiconductor package; and particularly to a semiconductor package, a semiconductor device and an electronic device which can be produced with ease, and a method for producing the semiconductor package.

Background Art

In recent years, a development of small-sized semiconductor devices has been promoted. With this development, attention is paid to the miniaturization of the packages of these semiconductor devices. For instance, a variety of semiconductor packages have been proposed in the August issue (1998) and February issue (1999) of Nikkei Micro-device. Among these packages, especially a wafer level CSP using a semiconductor package called CSP has a high effect on the miniaturization of a package and a reduction in costs. This CSP is a package resin-sealed together with a wafer. Fig. 15 is a sectional view showing the structure of a conventional CSP. Incidentally, Fig. 15 shows the condition that the above CSP will be mounted on a printed circuit board and the vertically positional relation between the parts explained hereinafter is reversed with respect to those of Fig. 15.

In the conventional CSP, plural electrodes, for example, Al pads 52 are formed on a wafer 51. Also a passivation film, for example, a SiN layer 53 and a **polyimide** layer 54 which cover the Al pads 52 are formed on the entire surface of the wafer 51. In the SiN layer 53 and the **polyimide** layer 54, a via hole which reaches the Al pad 52 from the surface of the **polyimide** layer 54 is formed and a conductive layer 55 is embedded in the via hole. On the **polyimide** layer 54, a rerouting layer 56 connected to the conductive layer 55 is formed. The rerouting layer 56 is formed of, for example, Cu. A sealing resin layer 57 coating the rerouting layer 56 is formed on the entire surface of the **polyimide** layer 54. Inside the sealing resin layer 57, a Cu post 58 which reaches the rerouting layer 56 from the surface of the sealing resin layer 57 is formed as a metal post. A barrier metal layer 59 is formed on the Cu post 58 and a solder ball 60 such as a solder is formed on the barrier metal layer 59.

Next, a method for producing the conventional CSP as mentioned above will be explained. Figs. 16 (a) to (e) are sectional views showing the method for producing the conventional CSP in step order. Incidentally, the rerouting layer, the **polyimide** layer and the like are omitted in Figs. 16 (a) to (e).

Firstly, as shown in Fig. 16 (a), a wafer 61 with a flat surface is prepared. As shown in Fig. 16 (b), plural Cu posts 62 are formed on the wafer 61 by plating. Next, as shown in Fig. 16 (c), all Cu posts 62 are resin-sealed such that they are encased to form a sealing resin layer 63. Then, as shown in Fig. 16 (d), the surface of the sealing resin layer 63 is polished to expose each Cu post 62. Thereafter, as shown Fig. 16 (e), a solder ball 64 such as a solder is mounted on each Cu post 62.

The CSP as described above is thus formed. This CSP is made into a given size by dicing afterwards.

Since a semiconductor package is in general different from a printed

circuit board or the like in thermal expansion coefficient, a stress based on the difference in thermal expansion coefficient focuses on a terminal of the semiconductor package. However, in the above-mentioned CSP, the stress is easily dispersed by making the cylindrical Cu post 62 have a large height.

However, in order to disperse the stress based on the difference in thermal expansion coefficient, it is necessary for a metal post, such as a Cu post, to have a height as large as about 100 (mu)m from the rerouting layer. However, if a metal post having such a height is formed by plating, there is a problem that a remarkable long period of time is required. This further gives rise to the problems of increased production cost and a difficulty in control of the height of the metal post.

In light of such problems, the present invention has been made. It is an object of the present invention to provide a semiconductor package, a semiconductor device and an electronic device which make it possible to disperse a stress produced when the package is mounted on a printed circuit board or the like and which can be produced for a short time, and a method for producing the semiconductor package.

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File : PLUSPAT

SS	Results	
1	0	..FAM US 20020066961/PN
2	8	(2) ..FAM JP4061194/PN
3	2	..CITB JP4061194/PN
4	2	..CITF JP4061194/PN
5	1	(1) ..FAM JP10150248/PN
6	1	..CITB JP10150248/PN
7	1	..CITF JP10150248/PN

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